Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of claims:

Claim 1 (currently amended). A method for testing a semiconductor memory having a plurality of memory banks, the testing involving test writing of information ~~being written~~ to memory addresses ~~and/or being read~~, reading the information from the memory addresses and checking whether the written information has been stored correctly, which comprises the steps of:

defining a plurality of subareas actuated independently of one another for a memory address array in each of the memory banks;

using first commands for accessing a first subarea of the memory address array in a respective memory bank and second commands for accessing a second subarea of the memory address array in the respective memory bank to form, for each of the memory banks, a compressed command sequence associated with the respective memory bank, the first commands being associated with uneven clock periods and the second commands

being associated with even clock periods ~~and being inserted between the first commands~~; and

test writing ~~and/or~~ and reading the information by executing in all of the memory banks respective compressed command sequences associated with the memory banks in parallel.

Claim 2 (original). The method according to claim 1, which further comprises:

dividing the memory address array in each of the memory banks into four subareas; and

forming the respective compressed command sequences such that in the uneven clock periods one of the first subarea and a third subarea and in the even clock periods one of the second subarea and a fourth subarea of the memory address array in the respective memory bank is accessed.

Claim 3 (original). The method according to claim 1, which further comprises defining an ordering of commands to alternately access a plurality of subareas of the memory address array in the respective memory bank within the respective compressed command sequences such that each clock

period has an associated command accessing one of the subareas of the respective memory bank.

Claim 4 (original). The method according to claim 1, which further comprises providing each of the respective compressed command sequences associated with a memory bank a succession of command blocks in which a command block contains commands for actuating a respective memory address from each of the subareas of the memory address array in the respective memory bank.

Claim 5 (original). The method according to claim 1, which further comprises providing each of the respective compressed command sequences with commands for one of writing the information and for reading the information and with further commands for one of activating word lines and deactivating the word lines.

Claim 6 (original). The method according to claim 2, which further comprises dividing the memory address array in each of the memory banks, in a direction perpendicular to a path of word lines, into a plurality of independently actuable subareas which are accessed alternately by the respective compressed command sequence associated with the respective memory bank.

Claim 7 (original). The method according to claim 1, which further comprises configuring the respective compressed command sequences associated with the memory banks such that each command for reading a memory address follows precisely two clock periods after a command which activates a word line to which the memory address to be read is connected.

Claim 8 (original). The method according to claim 1, which further comprises testing a dynamic semiconductor memory as the semiconductor memory.

Claim 9 (original). The method according to claim 1, which further comprises testing a dynamic read/write memory as the semiconductor memory.